REMARKS

Claims 1-26 and 30-32 are pending in the present application. Claims 1-27 and 30-33 were presented for examination. Claims 27 and 33 have been cancelled by amendment.

In the office action mailed May 28, 2003, the drawings were objected to under 37 C.F.R. 1.83(a). Claims 1-27 and 30-33 were rejected under 35 U.S.C. 112, first paragraph, and claims 1, 5, 8, 12, 25-27, 30, 32, and 33 were rejected under 35 U.S.C. 112, second paragraph. Claims 1-27 and 30-33 were further rejected under 35 U.S.C. 102(e) as being aniticipated by U.S. Patent No. 6,424,584 to Seyyedy ("the Seyyedy patent").

With respect to the objection to the drawings under 37 C.F.R. 1.83(a), claims 14, 20, 26, 30, and 32 have been amended to remove reference to "an external tester" and to "programmed programmable elements." However, the antifuse bank and antifuse address load commands recited in claims 26 and 32 are already shown in Figures 2, 4, 5, and 7. In Figures 4 and 7, the commands for loading bank and fuse address latches are shown in the timing diagrams as the signals applied to the data terminals (DQs). A table of example load commands are shown and discussed at page 7, lines 3-21, of the present application. Figure 5 illustrates an example of a suitable arrangement for the bank and fuse addresses, as well as the appropriate load commands to apply to the DQs of the device during test probe touchdown. In Figure 2, the DQs are shown as being coupled to the logic circuitry 350. As previously explained, the DQs represent the data terminals to which the bank and fuse latch load commands are applied, which are shown in the signal timing diagram of Figures 4 and 7. The description of each Figure further discloses the application of the load commands to the logic circuitry 350, and provides examples of the types of load commands and the organization of load commands. Thus, the limitation, "the logic circuitry receiving address load commands" is clearly shown in Figures 2, 4, 5, and 7. Consequently, the objection to the drawings under 37 C.F.R. 1.83(a) should be withdrawn.

With respect to the rejection of claims 1-27 and 30-33 under 35 U.S.C. 112, first paragraph, the Examiner is directed to Figure 4, and the description related to Figure 4, namely, page 8, line 27-page 10, line 28 of the present application. As described therein, the bank and fuse addresses are latched sequentially, in response to receiving a load bank address command and load fuse address command, respectively. For example, with respect to Figure 4, at a time

T0, the device at DUT0 is provided with the command "1". As shown in the table at page 7, lines 8-15, a command value "1" directs the device to load bank address banks 0 and 1. Thus, although at the time T0 the address signals applied to A0-An is applied to both bank address latches 330, 332 and the fuse address latches 340, 342, 344, 346, only the bank address latch 330 will latch the address because of the command 1. At a time T1, a new command "5" is provided to the device at DUT0, directing the device to load fuse address bank 0 (*see* table at page 7, lines 8-15). As a result, although at the time T1 the address signal representing a fuse address is applied to the bank address latches 330, 332 and the fuse address latches 340, 342, 344, 346, only the fuse address latch 340 will latch the address signals. The loading of bank and fuse addresses by the respective latches continues in this manner until the programming of the antifuses is complete. Figure 7 is a timing diagram illustrating an alternative embodiment of the present invention, but again, the bank and fuse address load commands are used to control which of the bank and fuse address latches 330, 332, 340, 342, 344, 346 will latch the address currently applied to the address terminals A0-An. Thus, the subject matter of claims 1-27 and 30-33 is described in the present application in such a way as to enable one skilled in the art to practice the invention.

The remaining issues under the Examiner's rejection of claims 1-27 and 30-33 under 35 U.S.C. 112, first paragraph, have been addressed by the previously discussed amendments to claims 14, 20, 26, 30, and 32, and the previous discussion with respect to the antifuse bank and antifuse address load commands recited in claims 26, 30, and 32. For the foregoing reasons, the rejection of claims 1-26 and 30-32 under 35 U.S.C. 112, first paragraph, should now be withdrawn. Claims 27 and 33 have been cancelled by amendment, and consequently, the rejection of these claims under 35 U.S.C. 112, first paragraph, is now moot.

With respect to the rejection of 1, 5, 8, 12, 25-27, 30, 32, and 33 under 35 U.S.C. 112, second paragraph, claims 1, 8, 26, 30, and 32 have been amended to overcome the Examiner's rejection. As previously mentioned, claims 27 and 33 have been cancelled, and consequently, the Examiner's rejection of claims 27 and 33 under 35 U.S.C. 112, second paragraph, is now moot.

With specific reference to the rejection of claim 32 for not having an antecedent basis for "the data terminals," the Examiner is directed to claim 32, line 7 to the limitation "data

terminals." This reference provides the antecedent basis for "the data terminals" limitation recited at line 16. Consequently, the rejection of claim 32 under 35 U.S.C. 112, second paragraph, should be withdrawn.

With specific reference to the rejection of claims 5, 12, and 25, the Examiner is directed to MPEP 2173.05(e). As stated therein, "[i]nherent components of elements recited have antecedent basis in the recitation of the components themselves. For example, the limitation 'the outer surface of said sphere' would not require an antecedent recitation that the sphere has an outer surface." *See* MPEP 2173.05(e), p. 2100-205, 8th ed., rev. 1. The limitation at issue, namely, "the completion," is an inherent component of the programming event. That is, the programming event, like all events, inherently has a completion, or a point at which the event ends. Consequently, the limitation "the completion of the programming event" is analogous to the example of the "sphere" and "the outer surface" provided in MPEP 2173.05(e). Thus, the antecedent basis for "the completion" is inherent in the recitation of "the programming event." Therefore, the rejection of claims 5, 12, and 25 under 35 U.S.C. 112, second paragraph, should be withdrawn.

It will be apparent from the previous comments that the amendments were made independent of the rejection of the claims to the cited references. None of previously mentioned amendments narrow or further limit the scope of the invention as recited by the respective claim. Generally, the amendments make explicit what is implicit in the claim, add language that is inherent in the unamended claim, or merely redefine a claim term that is previously apparent from the description in the specification. Consequently, the amendments should not be construed as being "narrowing amendments," because these amendments were not made for a substantial reason related to patentability.

As previously mentioned, claims 1-27 and 30-33 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Seyyedy patent.

The Seyyedy patent describes a redundancy antifuse bank for a memory device. In contrast to conventional antifuse banks, as described in the Background of the Invention, the antifuse bank described in the Seyyedy patent does not include circuitry dedicated to programming and comparing for *each* of the antifuses of the antifuse bank. Instead, the antifuse banks described in the Seyyedy patent share many comparing and programming elements

between the individual antifuses of an antifuse bank. For example, in comparing memory addresses with the addresses programmed in each of the antifuse banks, sense lines are precharged to a reference voltage, and in the event the memory address does not match the programmed address, the respective sense line will be coupled to a cell plate voltage level, and the voltage of the sense line will be pulled to voltage less than the reference voltage. As a result, a low BANK_MATCH signal will be generated indicating that the memory address does not match the programmed address. Conversely, if the memory address matches the programmed address, the sense line will remain isolated from the cell plate voltage, and maintain the precharge voltage. A high BANK_MATCH signal will be generated in response to indicate that an address match has been detected.

Claims 1, 8, 14, and 20 are patentably distinct from the Seyyedy patent. Claim 1 recites a method for programming programmable elements of a plurality of memory devices, each memory device having at least a first and second programmable element thereon, the method comprising programming the first programmable element of a first memory device of the plurality of memory devices, and programming the second programmable element of a second memory device of the plurality of memory devices, the programming of the first and second programmable elements overlapping at least for a period of time.

Claim 8 recites a method for programming programmable elements of a plurality of memory devices, comprising in a first memory device of the plurality of memory devices, latching a first address corresponding to a programmable element located at a first location on the memory devices, initiating a programming event to program the programmable element in the first memory device located at the first location, in a second memory device of the plurality of memory devices, latching a second address corresponding to a programmable element located at a second location on the memory devices, and before the completion of the programming event for the programmable element in the first memory device, initiating a programming event to program the programmable element in the second memory device located at the second location.

Claim 14 recites a method for programming programmable elements of a plurality of memory devices, comprising commanding a first of the memory devices to latch a first address corresponding to a programmable element located at a first location on the memory

devices, commanding a second of the memory devices to latch a second address corresponding to a programmable element located at a second location on the memory devices, and programming the programmable elements of the first and second of the memory devices substantially concurrently.

Claim 20 recites a method for programming antifuses of a plurality of memory devices, comprising providing to a first memory device of the plurality an address corresponding to a programmable element to be programmed in the first memory device, providing a load command to the first memory device to latch the address, providing to a second memory device of the plurality an address corresponding to a programmable element to be programmed in the second memory device, and providing a load command to the second memory device to latch the address.

The Examiner has failed to demonstrate that the Seyyedy patent discloses each limitation of the combination of limitations recited by claims 1, 8, 14, and 20. The Examiner has made reference to Figures 1, 2, 7, and 8, and col. 1, line 14, col. 3, lines 6-11, and col. 1, lines 23-48 of the Seyyedy patent as providing the basis for rejecting claims 1, 8, 14, and 20 under 35 U.S.C. 102(e). However, the material cited by the Examiner fails to describe the combination of limitations of claims 1, 8, 14, and 20. For example, the Seyyedy patent fails to disclose programming the first programmable element of a first memory device of the plurality of memory devices, and programming the second programmable element of a second memory device of the plurality of memory devices, the programming of the first and second programmable elements overlapping at least for a period of time. The Seyyedy patent discusses programming antifuses of one memory device, and does not mention programming antifuses of a second memory device where programming of the first and second memory devices overlaps at least for a period of time.

The Seyyedy patent also fails to disclose initiating a programming event to program the programmable element in the first memory device located at the first location, and before the completion of the programming event for the programmable element in the first memory device, initiating a programming event to program the programmable element in the second memory device located at the second location. As previously discussed, the Seyyedy patent does not mention programming of antifuses of two different memory devices. The

Seyyedy patent is directed to an antifuse bank where many of the comparing and programming elements are shared between the individual antifuses of an antifuse bank, rather than including circuitry dedicated to programming and comparing for each of the antifuses of the antifuse bank.

The Seyyedy patent also fails to disclose commanding a first of the memory devices to latch a first address corresponding to a programmable element located at a first location on the memory devices, commanding a second of the memory devices to latch a second address corresponding to a programmable element located at a second location on the memory devices, and programming the programmable elements of the first and second of the memory devices substantially concurrently. Additionally, the Seyyedy patent does not disclose providing to a first memory device of the plurality an address corresponding to a programmable element to be programmed in the first memory device, providing a load command to the first memory device to latch the address, providing to a second memory device of the plurality an address corresponding to a programmable element to be programmed in the second memory device, and providing a load command to the second memory device to latch the address. As previously discussed, the Seyyedy patent describes programming antifuses of one memory device, and does not address programming antifuses of two memory devices, or the overlap of programming time between two memory devices.

For the foregoing reasons, claims 1, 8, 14, and 20 are patentably distinct from the Seyyedy patent. Therefore, the rejection of claims 1, 8, 14, and 20 under 35 U.S.C. 102(e) should be withdrawn.

Claims 26, 30, and 32 are also patentably distinct from the Seyyedy patent. The Examiner's characterization of the functional blocks of Figures 7 and 8 of the Seyyedy patent are inaccurate, and do not illustrate elements analogous too the limitations recited by claims 26, 30, and 32. For example, the Examiner has characterized the control logic 224 as being representative of the logic circuitry recited in claims 26, 30, and 32. However, as illustrated in Figure 7 of the Seyyedy patent, the control logic 224 is not coupled to the data terminals of the memory device, unlike the logic circuitry recited in claims 26, 30, and 32. As described in the Seyyedy patent, the control logic 224 receives a clock signal (CLK) and COMMAND signal including CS, RAS, CAS, and WE signals, which are well known in the art as typical command signals for memory devices. *See* col. 8, lines 1-9. The Seyyedy patent does not describe the

control logic 224 coupled to the data terminals to receive antifuse bank and antifuse address load commands, unlike the logic circuitry recited in claims 26, 30, and 32.

The Seyyedy patent further fails to disclose the antifuse bank address and antifuse address latches recited in claims 26, 30, and 32. Although the Examiner has analogized the column and row address latches to the antifuse bank and antifuse address latches, the description found col. 8, lines 10-42 fails to describe the operation as recited in claims 26, 30, and 32. The Examiner has also characterized Figures 1 and 2 of the Seyyedy patent as disclosing programming circuitry capable of programming antifuses in the same manner as recited in claims 26, 30, and 32. However, the material describing Figures 1 and 2, namely, col. 1, line 64-col. 2, line 27, and col. 2, line 66-col. 3, lines 61, fails to describe the programming circuitry in the manner as characterized by the Examiner. For example, there is no discussion of overlapping programming of antifuses, concurrently or sequentially. The material merely describes conventional programming of antifuse or fuses for the purpose of remapping memory addresses to redundant memory.

For the foregoing reasons, claims 26, 30, and 32 are patentably distinct from the Seyyedy patent, and therefore, the rejection of claim 26, 30, and 32 under 35 U.S.C. 102(e) should be withdrawn.

Claims 2-7, which depend from claim 1, claims 9-13, which depend from claim 8, claims 15-19, which depend from claim 14, claims 21-25, which depend from claim 20, and claim 31, which depends from claim 30, are also patentably distinct from the Seyyedy patent based on their dependency from a respective allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. However, because each claim in an application represents a different invention, the rejection of an independent claim does not necessarily result in the rejection of claims depending therefrom. For the foregoing reasons, the rejection of claims 2-7, 9-13, 15-19, 21-25, and 31 under 35 U.S.C. 102(e) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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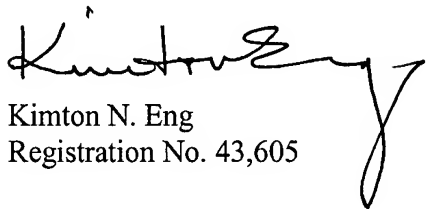

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